

REMARKS/ARGUMENTS

Claims 1-21 were pending. Claims 1, 5, 12, 13 and 16 have been amended, and no claims have been either added or canceled. Hence, claims 1-21 remain pending.

The Office Action of 10/25/06 rejects claims 1-5 and 9-21 under 35 U.S.C. 102(b) as being anticipated by Amick (U.S. Patent No. 6,650,157). Further, the Office Action of 5/4/2006 rejects claims 1-21 under 35 U.S.C. 102(e) as being anticipated by Masenas (U.S. Patent No. 6,525,615). Applicant respectfully traverses the rejection.

As amended, claim 1 provides a clock synthesizer including, *inter alia*, a phase interpolator that receives a pair of phases of a source clock, and is operable to combine the pair of phases of the source clock to generate the output clock signal that has at least one clock cycle inserted into the source clock signal. In this way, a frequency stepped up from the source clock is possible. Thus, in contrast to a pure PLL based clock synthesizer that provides a voltage feedback to a voltage controlled oscillator in order to increase or decrease a synthesized clock frequency to match an input clock signal, the invention as set forth in claim 1 inserts one or more additional clock pulses into an output clock stream to the frequency of the clock when compared with the input clock. An example of this is shown in Fig. 5a where Clk_{OUT} includes six positive clock pulses corresponding to the five positive clock pulses of phase P0 between times t1 and t6. Specification at p. 13, ll. 17-21 (“1 clock cycle is effectively inserted into the source clock over 12 source clock cycles to derive the output clock Clk_{OUT} with a stepped up frequency.”)

Amick fails to disclose, teach or suggest the invention as set forth in claim 1. Indeed, Amick explicitly teaches a circuit that is configured to “closely follow input characteristics”. Amick at col. 2, ll. 51-66. In particular, Amick provides for a phase shift, but maintains the same frequency as the input signal. Amick at col. 1, ll. 11-17. As such, Amick would not be expected to disclose, teach or suggest a circuit that specifically provides an output clock by modifying the frequency of an input clock. Accordingly, for at least the aforementioned reason, Applicant respectfully requests that the rejection based on Amick be withdrawn and claim 1 allowed.

Similarly, Masenas fails to disclose, teach or suggest the invention as set forth in claim 1. In particular, Masenas discloses a “phase selector within a digitally controlled phase-locked loop”. Masenas at Abstract. As with any phase-locked loop system, a control is provided to control frequency by providing a voltage or current feedback to a respective voltage controlled oscillator or a current controlled oscillator. Masenas at col. 5, ll. 11-17. Thus, in contrast to that set forth in claim 1, the phase interpolator specifically does not modify the frequency – that is done via the voltage controlled oscillator. Hence, for at least the aforementioned reason, Applicant respectfully requests withdrawal of the rejection of claim 1 based on Masenas.

As neither Amick nor Masenas discloses, teaches or suggests each limitation of claim 1, Applicant respectfully asserts that claim 1 is allowable over the cited art. Further, as claims 2-11 properly depend from allowable claim 1, Applicant respectfully requests withdrawal of the rejections of the aforementioned claims and allowance thereof.

As amended, claim 12 includes a limitation similar to that discussed above in relation to claim 1. Hence, for at least the reasons set forth in relation to claim 1 above, Applicant respectfully requests withdrawal of the rejection of claim 12 based on Amick and Masenas. Further, as claims 13-21 properly depend from allowable claim 12, Applicant respectfully requests withdrawal of the rejections of the aforementioned claims and allowance thereof.

CONCLUSION

In view of the foregoing, Applicant respectfully asserts that all claims now pending in the application are in condition for allowance. Hence, an early allowance of all such claims is earnestly requested.

Applicant herein files a Request for Continued Examination (RCE), and to the extent necessary Applicant petitions for an extension of time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees under 37 CFR 1.136, to the deposit account of the assignee, Texas Instruments Incorporated, Account No. 20-0668.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 720-266-4728.

Respectfully submitted,

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